WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor integrated circuit including:

a plurality of circuit modules;

a fuse circuit which has a plurality of nonvolatile memory cells capable of writing therein control information for defect relief, trimming of circuit characteristics or function switching with respect to the plurality of circuit modules and which allows memory information to be electrically read therefrom;

a dedicated wiring which allows the memory information of the fuse circuit to be transmitted to the circuit modules; and

testing external interface means which makes it possible to output information on the dedicated wiring to the outside of a semiconductor substrate and to externally input data to the dedicated wiring,

said method comprising:

a first process for supplying control information from the testing external interface means to each of the circuit modules through the dedicated wiring;

a second process for confirming an operation of each of the circuit modules in a supplied state of the control information; and

a third process for writing control data in the fuse circuit according to the result of confirmation by the second process.

2. A method of manufacturing a semiconductor integrated circuit according to claim 1, wherein the fuse circuit is concentratedly placed in one location of the semiconductor substrate.

3. A method of manufacturing a semiconductor integrated circuit according to claim 1, wherein the operation of the control circuit is started in response to an instruction for initializing the semiconductor integrated circuit.

4. A method of manufacturing a semiconductor integrated circuit according to claim 1, wherein the first register circuit and the plurality of second register circuits are connected in series by the second wiring.

5. A method of manufacturing a semiconductor integrated circuit according to claim 4, wherein the first register circuit is a shift register which holds control information parallel-outputted from the fuse circuit and outputs the same on a serial basis.

6. A method of manufacturing a semiconductor integrated circuit according to claim 5, wherein the second register circuits are shift registers which have serial input terminals connected upstream of the second wiring, serial output terminals connected downstream of the second wiring, and parallel output terminals connected to their corresponding circuit modules.

7. A method of manufacturing a semiconductor integrated circuit according to claim 1, further including testing external interface means which makes it possible to output information on the second wiring to the outside of the semiconductor substrate and to input data from outside to the second wiring.

8. A method of manufacturing a semiconductor integrated circuit according to claim 1, wherein the fuse circuit has a nonvolatile memory cell assigned for storage of a sign bit indicative of whether writing of control information into each of the nonvolatile memory cells is done.

9. A method of manufacturing a semiconductor integrated circuit according to claim 1, wherein the control information stored in the fuse circuit is any one of information for substituting a defective circuit module with a spare circuit module and control information for relieving a partial defect in each circuit module, or both information.

10. A method of manufacturing a semiconductor integrated circuit according to claim 1, wherein each of the nonvolatile memory cells includes:

nonvolatile memory elements having first source electrodes, first drain electrodes, floating gate electrodes and control gate electrodes and capable of having different threshold voltages;

read transistor elements having second source electrodes and second drain electrodes, having the floating gate electrodes as gate electrodes and capable of having mutual conductances different according to threshold voltages held by the nonvolatile memory elements; and

a selection transistor which connects the read transistor elements to a read signal line.

11. A method of manufacturing a semiconductor integrated circuit according to claim 1, wherein each of the nonvolatile memory cells includes:

nonvolatile memory elements having first source electrodes, first drain electrodes, floating gate electrodes and control gate electrodes and capable of having different threshold voltages;

read transistor elements having second source electrodes and second drain electrodes, having the floating gate electrodes as gate electrodes and capable of having switch states different according to threshold voltages held by the nonvolatile memory elements; and

a selection transistor which connects the read transistor elements to a read signal line.

12. A method of manufacturing a semiconductor integrated circuit according to claim 10, wherein each of the nonvolatile memory elements has a MOS capacitive element in which a capacitance electrode is provided over a first semiconductor region functioning as a control gate electrode with an insulating layer interposed there between, and a MOS transistor having a first source electrode, a first drain electrode and a gate electrode formed in a second semiconductor region, and the capacitance electrode is commonly connected to the gate electrode and functions as a floating gate electrode.

13. A method of manufacturing a semiconductor integrated circuit according to claim 10, wherein the nonvolatile memory elements and read transistor elements are respectively provided in pairs, and one read transistor element shares a floating gate electrode of one nonvolatile memory element, whereas the other read transistor element shares a floating gate electrode of the other nonvolatile memory element, and the pair of read transistor elements is series-connected to the selection transistor element.

14. A method of manufacturing a semiconductor integrated circuit according to claim 10, wherein the nonvolatile memory elements and read transistor elements are respectively provided in pairs, and one read transistor element shares a floating gate electrode of one nonvolatile memory element, whereas the other read transistor element shares a floating gate electrode of the other nonvolatile memory element, and the pair of read transistor elements is parallel-connected to the selection transistor element.

15. A method of manufacturing a semiconductor integrated circuit according to claim 11, wherein each of the nonvolatile memory elements has a MOS capacitive element in which a capacitance electrode is provided over a first semiconductor region functioning as a control gate electrode with an insulating layer interposed there between, and a MOS transistor having a first source electrode, a first drain electrode and a gate electrode formed

in a second semiconductor region, and the capacitance electrode is commonly connected to the gate electrode and functions as a floating gate electrode.

16. A method of manufacturing a semiconductor integrated circuit according to claim 11, wherein the nonvolatile memory elements and read transistor elements are respectively provided in pairs, and one read transistor element shares a floating gate electrode of one nonvolatile memory element, whereas the other read transistor element shares a floating gate electrode of the other nonvolatile memory element, and the pair of read transistor elements is series-connected to the selection transistor element.

17. A method of manufacturing a semiconductor integrated circuit according to claim 11, wherein the nonvolatile memory elements and read transistor elements are respectively provided in pairs, and one read transistor element shares a floating gate electrode of one nonvolatile memory element, whereas the other read transistor element shares a floating gate electrode of the other nonvolatile memory element, and the pair of read transistor elements is parallel-connected to the selection transistor element.